

Serial No. 10/690,629
Reply to Office Action of August 9, 2007

Docket No. GCTS-0036

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for reducing signal distortion in a receiver, comprising:
 - deriving a sequence of chips from a received signal;
 - canceling postcursor-inter-symbol interference (ISI) from the chip sequence to determine a current code complementary keying (CCK) codeword;
 - computing a chip-time reversed estimate of the current CCK codeword; and
 - canceling precursor-ISI from a previous CCK codeword based on the chip-time reversed estimate of the current CCK codeword.
2. (Original) The method of claim 1, wherein deriving the chip sequence includes:
 - convolving the received signal with coefficients of a channel matched filter.
3. (Original) The method of claim 1, further comprising:
 - generating terms for canceling the postcursor ISI from a chip sequence detected in a preceding symbol.
4. (Currently Amended) The method of claim 1, wherein canceling postcursor-ISI includes:
 - generating postcursor-ISI cancellation terms from a previously detected CCK chip sequence used to form a previous CCK codeword;
 - subtracting the ~~postcursor~~ postcursor-ISI cancellation terms from the chip sequence to produce a chip metric; and
 - determining said current CCK codeword using said chip metric.

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5. (Currently Amended) The method of claim 1, wherein canceling postcursor-ISI includes:

setting decision feedback equalizer (DFE) coefficients based on a previously detected CCK chip sequence;
generating postcursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock;
subtracting the postcursor-ISI terms from the chip sequence to produce a chip metric.

6. (Previously Presented) The method of claim 4, wherein the current CCK codeword is generated by inputting said chip metric into a CCK correlator.

7. (Currently Amended) The method of claim 1, wherein canceling the precursor-ISI includes:

computing conjugates of chip values of a future symbol;
setting decision feedback equalizer (DFE) coefficients based on the conjugates;
generating precursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock; and
subtracting the precursor-ISI terms from chip metrics corresponding to the previous CCK codeword.

8. (Currently Amended) The method of claim 1, wherein the received signal is one generated in a direct-sequence spread-spectrum (DSSS/CCK) wireless communications system.

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9. (Original) The method of claim 1, further comprising:
equalizing signal energy in a codeword correlator bank used to generate the
current and previous CCK codewords.
10. (Original) The method of claim 1, further comprising:
(a) obtaining chips of the previous CCK codeword generated after
cancellation of the precursor-ISI; and
(b) performing postcursor-ISI and precursor-ISI based on the previous
CCK codeword chips obtained in (a).
11. (Original) The method of claim 10, further comprising:
repeating steps (a) and (b) a predetermined number of times.
12. (Currently Amended) A system for reducing signal distortion in a receiver,
comprising:
channel matched filter which generates a sequence of chips from a received
signal;
a decision feedback equalizer (DFE) which cancels postcursor-inter-symbol
interference (ISI) from the chip sequence to produce a chip metric; and
a code complementary keying (CCK) correlation-decision block which
generates a current CCK codeword based on said chip metric, wherein the DFE cancels
precursor-ISI from a previous CCK codeword based on a chip-time reversed estimate of the
current CCK codeword.
13. (Original) The method of claim 12, wherein the DFE cancels postcursor-ISI

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by generating postcursor-ISI correction terms from a previously detected CCK chip sequence used to form the previous CCK codeword and subtracting the postcursor-ISI correction terms from the chip sequence to produce said chip metric.

14. (Original) The system of claim 12, wherein the DFE cancels postcursor-ISI by setting DFE coefficients based on a previously detected CCK chip sequence, generating postcursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock, and subtracting the postcursor-ISI terms from the chip sequence to produce said chip metric to produce said chip.

15. (Original) The system of claim 12, wherein the DFE cancels the precursor-ISI by computing conjugates of chip values of a future symbol, setting DFE coefficients based on the conjugates, generating precursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock, and subtracting the precursor-ISI terms from chip metrics corresponding to the previous CCK codeword.

16. (Original) The system of claim 12, wherein the receiver is a DSSS/CCK wireless communications receiver.

17. (Original) The system of claim 12, further comprising:
an energy bias canceler which equalizes signal energy in the codeword correlator bank.

18. (Currently Amended) A bidirectional turbo inter-symbol interference (ISI) canceler (BTIC), comprising:
a single-symbol detector which generates a sequence of chips from a received

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signal;

a postcursor-ISI canceler to ~~generate postcursor-ISI cancellation terms from a previously detected chip sequence used to form a previous code complementary keying (CCK) codeword and to cancel postcursor-ISI from the chip sequence to output a representation of said postcursor-ISI~~ produce a chip metric; and

a precursor-ISI canceler to ~~cancel~~ generate precursor-ISI cancellation terms based on a chip-time reversed estimate of a current CCK codeword generated from said chip metric to cancel precursor-ISI from the previous CCK codeword ~~said representation of said postcursor-ISI~~.

19. (Currently Amended) The bidirectional turbo ISI canceler of claim 18, wherein the single-symbol detector includes a RAKE receiver, ~~wherein said pre-cursor-ISI canceler cancels said precursor-ISI based on a chip time reversed estimate of a current CCK codeword generated from said representation of said postcursor-ISI.~~

20. (Currently Amended) The bidirectional turbo ISI canceler of claim 18, ~~wherein the single-symbol detector includes comprising:~~

a channel matched filter which generates the chip sequence from the received signal; and

a codeword correlator bank which generates ~~the~~ a current CCK codeword from said representation of said postcursor-ISI.

21. (Original) The bidirectional turbo ISI canceler of claim 20, wherein the single-symbol detector further includes an energy bias canceler to equalize signal energy in the codeword correlator bank.

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22. (Currently Amended) A method for reducing distortion in a receiver, comprising:

- computing a set of decision feedback equalizer (DFE) coefficients;
- canceling postcursor- inter-symbol interference (ISI) caused by a preceding symbol using the set of DFE coefficients; and
- canceling precursor-ISI caused by a trailing symbol using the same set of DFE coefficients.

23. (Currently Amended) A receiver, comprising:

- a first feedback canceler ~~which cancels to cancel~~ postcursor- inter-symbol interference (ISI) caused by a preceding symbol;
- a second feedback canceler ~~which cancels to cancel~~ precursor-ISI caused by a trailing symbol, wherein the first and second feedback cancellers use a same set of decision feedback equalizer (DFE) coefficients to cancel the postcursor-ISI and precursor-ISI.

24. (Currently Amended) The receiver of claim 23, wherein the first and second feedback cancellers are included in ~~a same at least one DFE, the second feedback canceller to use the set of DFE coefficients being time-reversed to cancel the precursor-ISI.~~

25. (New) The method of claim 22, wherein said canceling postcursor-ISI and the canceling precursor-ISI are respectively performed in first and second feedback canceler units based on the set of DFE coefficients.